

Docket No. 200209168-1

Remarks

This Amendment is responsive to the April 20, 2006 Office Action. Reexamination and reconsideration of claims 1-54 is respectfully requested.

Summary of The Office Action

Claims 1, 3-11, 19-21, 23-27, 29-32, 35-44, and 47-54 were rejected under 35 U.S.C. §102(b) as being anticipated by Hayasaki (EP 1128324).

Claims 2, 22, and 28 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hayasaki (EP1128324) in view of Axtell et al. (US 20020060722).

Claims 12-18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hayasaki (EP 1128324) in view of Cleland et al. (US 6491377).

Claims 33, 34, 45, and 46 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hayasaki (EP 1128324).

The Amendment

Independent claim 35 has been amended to include language from dependent claim 37. Thus, no new matter has been added. Accordingly, claim 37 is now cancelled.

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The Claims Patentably Distinguish Over the References of Record

Claims 1, 3-11, 19-21, 23-27, 29-32, 35-44, and 47-54 were rejected under 35 U.S.C. §102(b) as being anticipated by Hayasaki (EP 1128324).

35 U.S.C. §102

For a 35 U.S.C. §102 reference to anticipate a claim, the reference must teach every element of the claim. Section 2133 of the MPEP recites:

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Independent Claim 1

Claim 1 was rejected under 35 U.S.C. §102 as being anticipated by Hayasaki. Applicant respectfully submits that Hayasaki does not anticipate claim 1. Claim 1, lines 6-8 recite, "a first address generator configured to provide first address signals; a second address generator configured to provide second address signals." The Office Action states, on page 2, that "Hayasaki teaches a first address generator configured to provide first address signals; a second address generator configured to provide second address signals (figure 3, element 8'; [0058-0060])." Thus, the rejection is based on element 8' and paragraphs [0058-0060].

However, Applicant respectfully submits that element 8' is a 44-bit Latch that holds data, not addresses. Thus, Latch 8' is not an address generator and does not teach or suggest "a first address generator configured to provide first address signals" or "a second address generator configured to provide second address signals."

In particular referring to Figure 3, Hayasaki teaches data signals DATA0-DATA3 are inputted to Latch 8'. The corresponding specification makes no discussion of address signals. Rather, Hayasaki discloses data signals:

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“Four-bit data input from the four data signal lines DATA0 to DATA3 are sequentially input to the 4-bit shift register 4 and 4 x 11-bit shift register 8, and then held in 3-bit latch 4’ and 44-bit latch 8’.” (paragraph [0064]) (emphasis added).

Thus, the signals going into and the signals being output from the Latch 8’ are data signals, not address signals. Accordingly, latch 8’ is not an address generator. Therefore, Hayasaki fails to teach or suggest a first or second address generator and fails to support the §102 rejection.

Looking more closely to Figure 3 and tracing the circuit, Hayasaki teaches that the data signals DATA0-DATA3 ultimately become input to Latch 4’ and Latch 8’. Thus, these components and signal lines process data signals, and do not generate address signals. The Hayasaki specification supports this reading since it teaches:

“...a 4-bit shift register 4 for sequentially holding input 4-bit data signals, a 44-bit latch 8’ for holding printing data for the 44 printing elements in a block, and a 4 x 11-bit shift register 8 for sequentially holding 11 input 4-bit data signals.” (paragraph [0060]) (emphasis added).

Hayasaki clearly discloses that Latch 8’ holds and outputs “printing data,” not address signals. Thus, latch 8’ is not an address generator.

Accordingly, Hayasaki does not anticipate each and every element of claim 1 and fails to establish a proper §102 rejection. The rejection should thus be withdrawn. As such, dependent claims 2-20 also are not taught or suggest by the reference and patentably distinguishes over the references of record.

Dependent Claims 3-10

Claims 3-10 depend from claim 1 and were also rejected under 35 U.S.C. §102(b) as being anticipated by Hayasaki. Claims 3-10 recite various limitations relating to the first or second address generators, and/or the first or second address signal lines. Since Hayasaki fails to teach or suggest first or second address generators, Hayasaki further fails to teach or suggest the particular limitations from claims 3-10.

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Therefore, Hayasaki fails to support a proper §102 rejection with respect to these claims for this additional reason and the rejection must be withdrawn.

Independent Claim 21

Independent Claim 21 was rejected under 35 U.S.C. §102(b) as being anticipated by Hayasaki (EP 1128324). The Office Action on page 6 cites to Hayasaki Figure 3, element 8' and paragraphs [0058-0060] as teaching the recited means for generating first address signals and the means for generating the second address signals of claim 21.

Based on the above discussions of Hayasaki and the teachings of the circuit from Figure 3, element 8' is a latch that holds printing data, not address signals. Furthermore, all the elements in the circuit of Figure 3 that are connected to the DATA0-DATA3 lines process data, not address signals. Therefore, no element in Hayasaki (including latch 8') teaches or suggests means for generating address signals. Claim 21 thus patentably distinguishes over the references of record.

Accordingly, Hayasaki fails to establish a proper §102 rejection and the rejection must be withdrawn. It then follows that dependent claim 22-25 also patentably distinguish over the references of record and are in condition for allowance.

Dependent Claims 23-25

Claims 23-25 depend from claim 21 and were also rejected under 35 U.S.C. §102(b) as being anticipated by Hayasaki. Claims 23-25 recite various limitations relating to the means for generating address signals, and/or first or second address signals. Since Hayasaki fails to teach or suggest a means for generating address signals, Hayasaki further fails to teach or suggest the particular limitations of claims 23-25.

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Therefore, Hayasaki fails to support a proper §102 rejection with respect to these claims for this additional reason and the rejection must be withdrawn.

Independent Claim 26

Independent Claim 26 was rejected under 35 U.S.C. §102(b) as being anticipated by Hayasaki. The Office Action on page 7 cites to Hayasaki Figure 3, element 8' and paragraphs [0058-0060] as teaching the recited elements of generating first address signals and generating second address signals, and other limitations relating to the address signals.

It has been shown that Hayasaki teaches elements that process printing data. Element 8' is a data latch that holds printing data, not address signals. Hayasaki fails to disclose generating address signals and no method has been shown that includes generating address signals as claimed.

Accordingly, Hayasaki fails to establish a proper §102 rejection and the rejection must be withdrawn. Claim 26 thus patentably distinguishes over the references of record. It then follows that dependent claim 27-34 also patentably distinguish over the references of record and are in condition for allowance.

Independent Claim 35

Independent Claim 35 was rejected under 35 U.S.C. §102(b) as being anticipated by Hayasaki. The Office Action on page 8 cites to Hayasaki Figure 3, element 8' and paragraphs [0058-0060] as teaching the recited first source of address signals. For the reasons set forth above, Hayasaki fails to teach or suggest a first source of address signals and thus fails to establish a proper §102 rejection. The rejection should be withdrawn and claim 35 be allowed. Accordingly, dependent claims 36 and 38 should also be in condition for allowance.

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Independent Claims 39, 43, 48-54

Independent Claims 39, 43, 48-54 were also rejected under 35 U.S.C. §102(b) as being anticipated by Hayasaki. These claims recite various features relating to address generators and/or address signals. Each claim should be reviewed to identify the particular features recited. It has been shown that Hayasaki teaches elements that process data from DATA0-DATA3 lines and fails to mention any feature related to address generators or address signals. Therefore, Hayasaki fails to teach each and every element of these claims. The rejection is thus not supported and must be withdrawn.

Accordingly, claims 39-54 including their dependent claims, patentably distinguish over the references of record and are in condition for allowance.

The §103 Rejections

All the §103 rejections were based on the primary reference of Hayasaki as follows:

Dependent Claims 2, 22, 28 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hayasaki in view of Axtell.

Dependent Claims 12-18 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hayasaki in view of Cleland.

Dependent Claims 33, 34, 45, 46 were rejected under 35 U.S.C. §103(a) as being unpatentable over Hayasaki.

Since Hayasaki fails to teach or suggest each and every limitation of the independent claims as explained above, Hayasaki also fails to support a proper §103 rejection and the rejection must be withdrawn. The combined references thus fail to cure the short comings of Hayasaki as related to the independent claims and do not establish a proper obviousness rejection as related to the dependent claims. Accordingly, all dependent claims patentably distinguish over the references of record and are in condition for allowance.

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Conclusion

For the reasons set forth above, **claims 1-36 and 38-54** patentably and unobviously distinguish over the references and are allowable. An early allowance of all claims is earnestly solicited.

Respectfully submitted,



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